[This question paper contains 4 printed pages.]

Not For Visually handicapped Students

Sr. No. of Question Paper : 1774 GC-3 Your Roll No. 16058...

Unique Paper Code : 32341102

Name of the Paper : Computer Systems Architecture

Name of the Course : **B.Sc. (H) Computer Science**

Semester : I

Duration : 3 Hours Maximum Marks : 75

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Attempt **all** questions from **Section A.**
3. Attempt any **four** questions from **Section B.**
4. Attempt **all** parts of a question together.

SECTION – A

1. (a) Simplify the following Boolean function F together with don't care conditions d in (i) sum of product and (ii) product of sums form.

$F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10)$

$d(w, x, y, z) = \Sigma(5, 6, 11, 15)$ (5)

(b) Perform the arithmetic operations (+45) + (–17) and (–45) – (–17) in binary using 2's complement representation for negative numbers. (5)

(c) Draw a flowchart depicting the instruction cycle of basic computer. (5)

P.T.O.

(d) The system with micro-programmed control unit is having control memory of 2048 words of 32 bits each. The micro-instruction has three fields as shown below :

Micro-operation field	Select status bits	Branch address
16	5	11

How many bits are there in branch address field and if there are 32 status bits in the system, how many bits are used to select a status bits. How many bits are there in micro-operation field ? (5)

(e) Explain relative addressing mode with an example. Also give the advantage of relative addressing mode. (5)

(f) Give the space-time diagram for four segment pipeline 6 tasks and explain. Also calculate speedup ratio for pipeline. (5)

(g) Explain direct mapping in cache memory with the help of an example. Draw a well labeled diagram of the process. (5)

SECTION – B

2. (a) Draw the logic diagram of 3 × 8 decoder and explain its functioning. (5)

(b) Design a two bit counter with two flip-flops and one input x. When x = 0, the state of flip-flops does not change. When x = 1, the state sequence is 00, 01, 10, 11, 00 and repeat. (5)

3. (a) Show the contents (in hexadecimal) of registers PC, AR, DR. IR and SC of the basic computer when an LDA instruction is fetched from the memory and

executed. The initial content of PC is 7FF. The content of memory at address 7FF is AA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. Show the contents of registers in a tabular format. (5)

(b) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of the seven addressing modes, a register address field to specify one of the 64 registers, and a memory address. Specify the instruction format and the number of bits in each field assuming 32-bit instruction. (5)

4. (a) Convert following postfix expressions into infix expressions : (5)

(i) A B C D E + * -/

(ii) A B C * / D – E F / +

(b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed-up ratio of the pipeline for 100 tasks. What is the maximum achievable speed-up ? (5)

5. (a) Explain the organization of a micro programmed control unit with the help of a block diagram. (5)

(b) What is Content Addressable Memory ? Give an application of this memory. (5)

6. (a) Show the step-by-step multiplication process using Booth algorithm for the following numbers in binary : (+15) × (–12). (5)

P.T.O.

(b) Give the block diagram of DMA and discuss its functioning. (5)

7. (a) Distinguish between isolated I/O and memory mapped I/O. (5)

(b) What is hit-ratio with reference to cache memory ? Relate it to property of locality of reference. (5)